

# PI2PCIE412-D

# Enhanced, 1.8V, PCI Express Compliant, 4-Differential Channel, 2:1 Mux/DeMux Switch, w/ Single Enable

# Features

- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express signal compliance
- Low Bit-to-Bit Skew, 10ps max (between '+' and '-' bits)
- Low Crosstalk: -65dB@10 MHz
- Low Off Isolation: -65dB@10 MHz
- V<sub>CC</sub> Operating Range: +1.5V to +2.0V
- ESD Tolerance: 8kV HBM I/O; 2kV HBM select pin
- Low channel-to-channel skew, 35ps max
- Packaging (Pb-free & Green): – 42-contact, TQFN (ZH42)

**Block Diagram** 

# Description

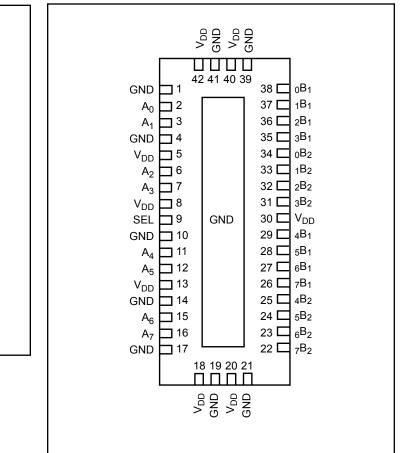
Pericom Semiconductor's PI2PCIE412-D is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express lanes to one of two locations. Using a unique design technique, Pericom has been able to minimize the impedance of the switch such that the attenuation observed through the switch is negligible. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification.

# Application

Switch a PCI-Express lane output between two PCI Express lane inputs.

# **Pin Description**

1



#### $_0B_1$ A<sub>0</sub> A<sub>1</sub> 1B1 $A_2$ <sub>2</sub>B<sub>1</sub> $A_3$ 3B1 $_0B_2$ $_1B_2$ <sub>2</sub>B<sub>2</sub> 3B2 <sub>4</sub>B<sub>1</sub> $A_4$ $_5B_1$ $A_5$ <sub>6</sub>B<sub>1</sub> $A_6$ 7B1 A7 $_{4}B_{2}$ <sub>5</sub>B<sub>2</sub> <sub>6</sub>B<sub>2</sub> <sub>7</sub>B<sub>2</sub> SEL

# **Truth** Table

Function	SEL
A <sub>N</sub> to <sub>N</sub> B <sub>1</sub>	L
$A_N$ to $_NB_2$	Н



# **Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	65°C to +150°C
Supply Voltage to Ground Potential	0.5V to +2.5V
DC Input Voltage	–0.5V to V <sub>CC</sub>
DC Output Current	120mA
Power Dissipation	0.5W

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# **DC Electrical Characteristics for Switching over Operating Range** ( $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CC} = 1.5V$ to 2.0V)

Paramenter	Description	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed HIGH level	$0.65 \text{ x V}_{CC}$			
V <sub>IL</sub>	Input LOW Voltage	Guaranteed LOW level	-0.5		$0.35 \mathrm{~x~V_{CC}}$	V
V <sub>IK</sub>	Clamp Diode Voltage	$V_{CC} = Max., I_{IN} = -18mA$		-0.7	-1.2	
IIH	Input HIGH Current	$V_{CC} = Max., V_{IN} = V_{CC}$			±5	
IIL	Input LOW Current	$V_{CC} = Max., V_{IN} = GND$			±5	μΑ

# **Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
I <sub>CC</sub>	Quiescent Power Supply Current	$V_{CC} = Max., V_{IN} = GND \text{ or } V_{CC}$		200		μA

#### **Dynamic Electrical Characteristics Over the Operating Range** (T<sub>A</sub>= -40° to +85°C, V<sub>CC</sub> = 1.8V±10%, GND=0V)

Parameter	Description	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max.	Units
X <sub>TALK</sub>	Crosstalk	See Fig. 1 for Measurement Setup, $f = 10 \text{ MHz}$		-65		dB
O <sub>IRR</sub>	OFF Isolation	See Fig. 2 for Measurement Setup, $f = 10 \text{ MHz}$		-65		uВ

#### Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 1.8V$ ,  $T_A = 25^{\circ}C$  ambient and maximum loading.



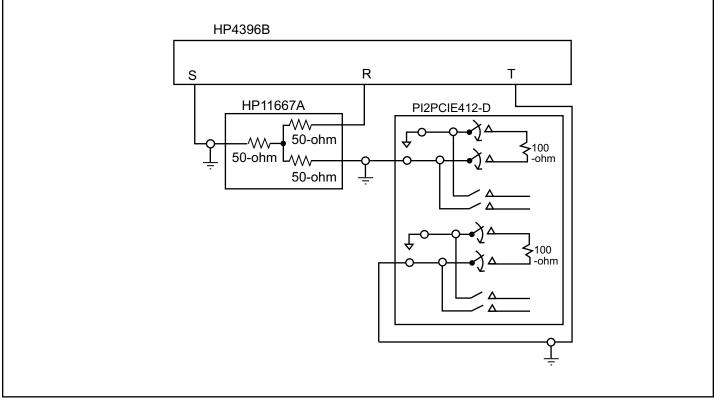


Fig 1. Crosstalk Setup

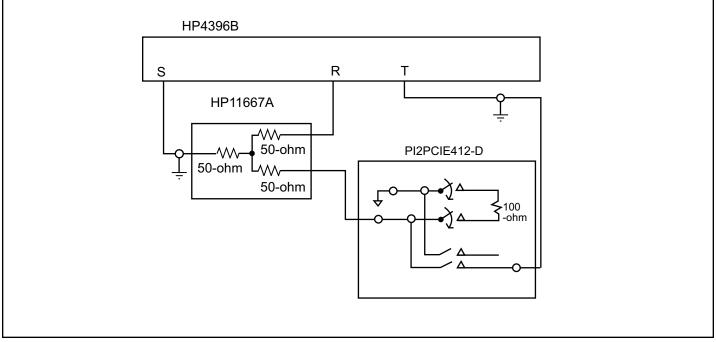


Fig 2. Off-isolation setup



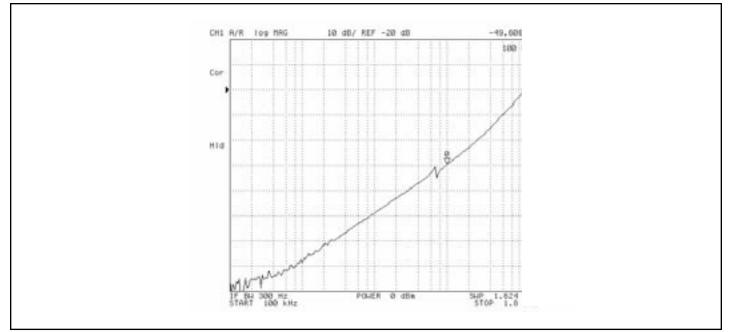


Fig 3. Crosstalk

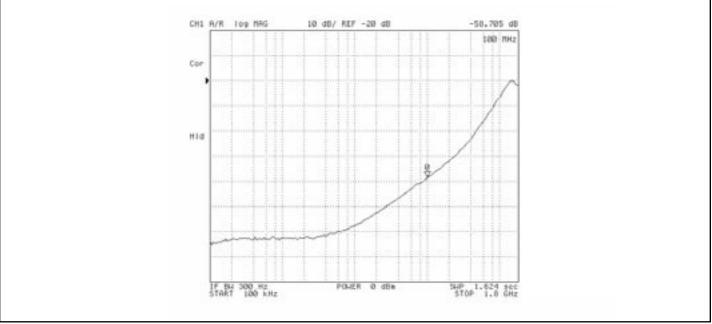


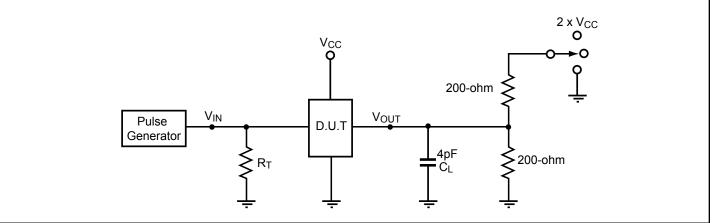
Fig 4. Off Isolation



# Switching Characteristics ( $T_A$ = -40° to +85°C, $V_{CC}$ = 1.8V±10%)

Paramenter	Description		Max.	Units	
tpZH, tpZL	Line Enable Time - SEL to A <sub>N</sub> , B <sub>N</sub>	0.5	8.0	na	
tPHZ, tPLZ	Line Disable Time - SEL to A <sub>N</sub> , B <sub>N</sub>	0.5	4.0	4.0 ns	
t <sub>b-b</sub>	Bit-to-bit skew within the same differential pair		10	ps	
tch-ch	Channel-to-channel skew		35	ps	

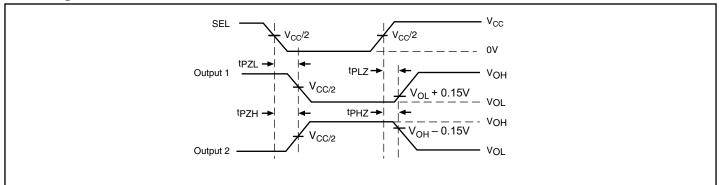
# **Test Circuit for Electrical Characteristics**<sup>(1-5)</sup>



#### Notes:

- 1.  $C_L$  = Load capacitance: includes jig and probe capacitance.
- 2.  $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator
- 3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. All input impulses are supplied by generators having the following characteristics: PRR  $\leq$  MHz, Z<sub>O</sub> = 50 $\Omega$ , t<sub>R</sub>  $\leq$  2.5ns, t<sub>F</sub>  $\leq$  2.5ns.
- 5. The outputs are measured one at a time with one transition per measurement.

# **Switching Waveforms**



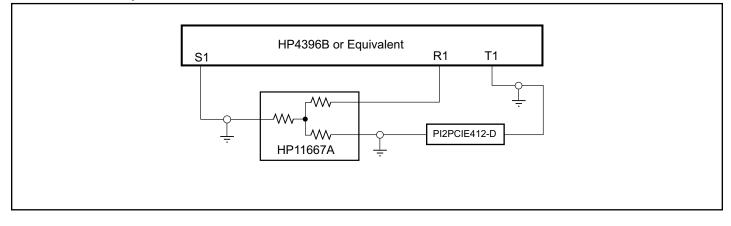
#### **Voltage Waveforms Enable and Disable Times**

# Switch Positions

Test	Switch
t <sub>PLZ</sub> , t <sub>PZL</sub> (output on B-side)	2 x V <sub>CC</sub>
t <sub>PHZ</sub> , t <sub>PZH</sub> (output on B-side)	GND
Prop Delay	Open



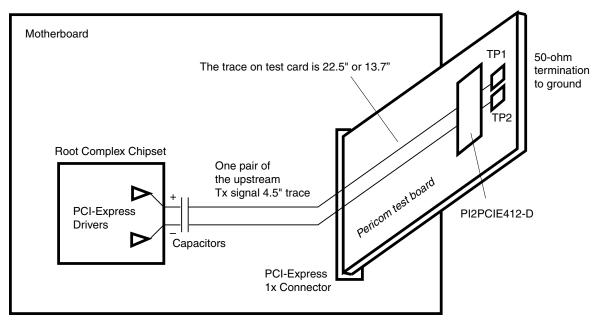
# **Test Circuit for Dynamic Electrical Characteristics**



# **Applications Information**

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd

# PCI Express Application Specific Measurements and Test Set-up



# **Figure 5: Test Setup**



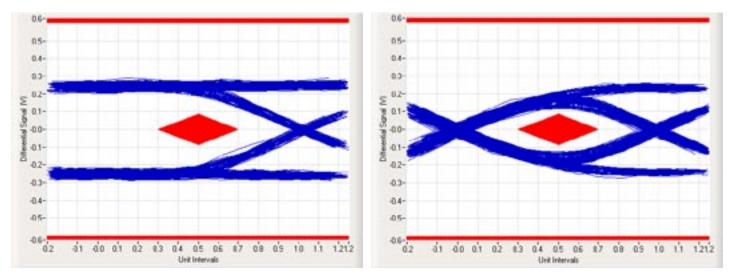


Figure 6: The worst non-transition signal eye (left) and the worst transition signal eye (right) of the PCI-SIG compliance software test using PI2PCIE412-D + 22.5" test card

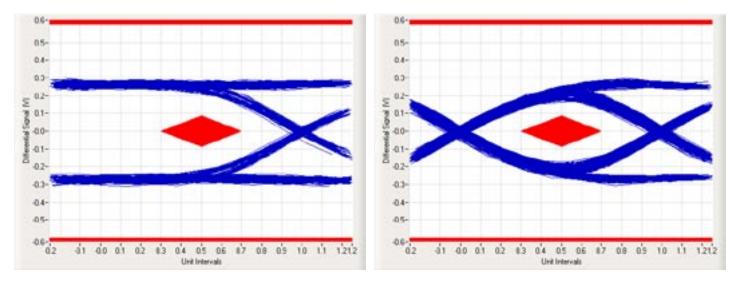


Figure 7. The worst non-transition signal eye (left) and the worst transition signal eye (right) of the PCI-SIG compliance software test with no switch + w/ 22.5" test card



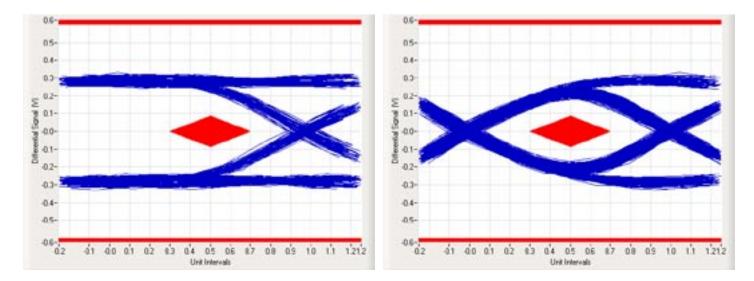


Figure 8: The worst non-transition signal eye (left) and the worst transition signal eye (right) of the PCI-SIG compliance software test using PI2PCIE412-D + 13.7" test card

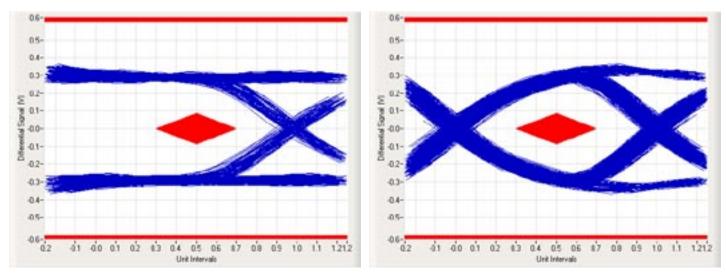
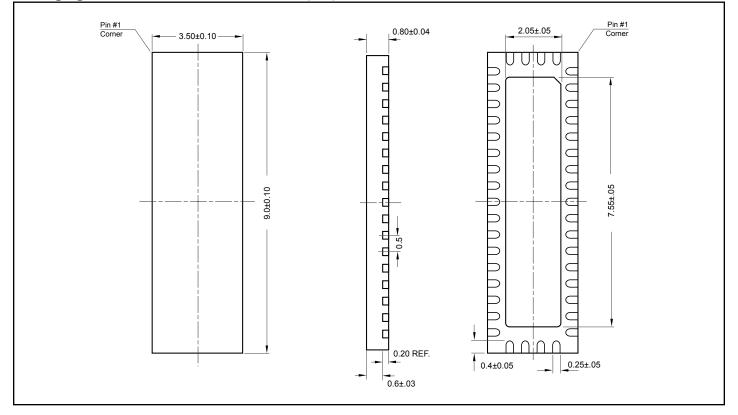


Figure 9: The worst non-transition signal eye (left) and the worst transition signal eye (right) of the PCI-SIG compliance software test with no switch + 13.7" test card



# PI2PCIE412-D Enhanced, 1.8V, PCI Express Compliant, 4-Differential Channel, 2:1 Mux/DeMux Switch

# Packaging Mechanical: 42-Contact TQFN (ZH)



# **Ordering Information**

Ordering Code	Package Code	Package Description
PI2PCIE412-DZHE	ZH	Pb-free & Green, 42-contact TQFN

#### Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• "E" denotes Pb-free and Green

• Adding an "X" at the end of the ordering code denotes tape and reel packaging